## REMARKS/ARGUMENTS

In view of the foregoing amendments and the following remarks, reconsideration of this application is requested. Claims 1-6 and 9-11 are now pending with claims 1 and 9 being independent.

Claim 1 describes a method of performing a product operation with rounding in a microprocessor in response to a single rounding multiplication instruction. The method includes fetching a first pair of elements and a second pair of elements. The method also includes forming a most significant product of a first element of the first pair of elements and a most significant element of the second pair of elements and a least significant product of the first element of the first pair of elements and a least significant element of the second pair of elements. The method further includes combining the most significant product with the least significant product to form a combined product, wherein combining comprises shifting the most significant product left by a width of the least significant element of the second pair of elements prior to adding the most significant product to the least significant product. The method also comprises rounding the combined product to form an intermediate result and shifting the intermediate result a selected amount to form a final result.

Claims 1-6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman (U.S. Patent No. 6,014,684) in view of either Balkanski et al (record reference) or Saishi et al. (record reference). Applicant requests reconsideration and withdrawal of these rejections for at least the reason that none of the references describes or suggests fetching a first pair of elements and a second pair of elements and forming a most significant product of a first element of the first pair of elements and a most significant element of the second pair of elements and a least significant product of the first element of the first pair of elements and a least significant element of the second pair of elements. Furthermore, none of the references describes or suggests shifting the most significant product left by a width of the least significant element of the second pair of elements prior to adding the most significant product to the least significant product.

Hoffman, in relevant part, describes in the Abstract, Cols. 1-2, and Figure 1 performing N-bit by 2*N bit multiplication. Figure 1 in Hoffman shows a value A of length 2*N-bits and a value B of length N-bits. The value A is divided into a most significant half ($A_{HIGH}$) and a least

significant half ($A_{LOW}$). In step 110, $A_{HIGH}$ is multiplied by B using unsigned multiplication to generate $B*A_{HIGH}$. In step 120, $A_{LOW}$ is multiplied by B using unsigned multiplication to generate $B*A_{LOW}$. The result $B*A_{HIGH}$ is logical shifted left by K bits in step 130. The result $B*A_{LOW}$ is arithmetic shifted right by (N-K) bits in step 140. Adding the shifted $B*A_{HIGH}$ and $B*A_{LOW}$ in step 150 yields B*A.

In Hoffman, a value B of length N-bits is multiplied by a value A of length 2*N-bits. Hoffman does not describe or suggest fetching a first pair of elements and a second pair of elements. Value B is an element of length-N bits and is not a first pair of elements of length 2*N-bits. Thus, Hoffman does not describe or suggest forming a most significant product of a first element of the first pair of elements (as only element B is described) and a most significant element of the second pair of elements and a least significant product of the first element of the first pair of elements and a least significant element of the second pair of elements.

Hoffman also does not describe or suggest shifting the most significant product left by a width of the least significant element of the second pair of elements prior to adding the most significant product to the least significant product. In Hoffman, as shown in Figure 1, the most significant product $B*A_{HIGH}$ is logical shifted left by K bits in step 130 and not by the width N of the least significant element $A_{LOW}$ of the second pair of elements $A_{HIGH}A_{LOW}$. In Hoffman, as described in column 2, lines 8-19, logical shift step 130 and arithmetic shift step 140 result in aligning the least significant bit position of $B*A_{HIGH}$ with the (N+1) least significant bit position of $B*A_{LOW}$. Thus, Hoffman does not describe or suggest shifting the most significant product left by a width of the least significant element of the second pair of elements prior to adding the most significant product to the least significant product.

Balkanski teaches a digital video compression system and an apparatus having a "rounding" system. Column 9 describes a 16-bit by 16-bit multiplier for multiplying the 16-bit inputs to generate a 32-bit result. The number represented by bits 31 through 15 is rounded up by adding a 1 at bit position 14. Balkanski fails to remedy the failure of Hoffman to describe or suggest fetching a first pair of elements and a second pair of elements and forming a most significant product of a first element of the first pair of elements and a most significant element of the second pair of elements and a least significant product of the first element of the first pair of elements and a least significant element of the second pair of elements. Balkanski further fails

to remedy the failure of Hoffman to describe or suggest shifting the most significant product left by a width of the least significant element of the second pair of elements prior to adding the most significant product to the least significant product.

Saishi teaches a multiplication method and a multiplication circuit, wherein a multiplicand is multiplied by a multiplier using a multiplication process, the result of the multiplication is added by an addition process to a rounding signal to be output from a rounding signal generation process, and the result of the addition, i.e., a multiplication result obtained after rounding, is stored in a register. Saishi fails to remedy the failure of Hoffman to describe or suggest fetching a first pair of elements and a second pair of elements and forming a most significant product of a first element of the first pair of elements and a most significant element of the second pair of elements and a least significant product of the first element of the first pair of elements and a least significant element of the second pair of elements. Saishi further fails to remedy the failure of Hoffman to describe or suggest shifting the most significant product left by a width of the least significant element of the second pair of elements prior to adding the most significant product to the least significant product.

Claims 2-6 depend from independent claim 1. Accordingly, Applicant requests that the rejections of claims 2-6 over the Hoffman, Balkanski, and Saishi references be withdrawn for the reasons discussed above with respect to claim 1.

Claim 6 describes wherein the first element of the first pair of elements is a most significant element of the first pair of elements. Claim 6 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman in view of either Balkanski et al (record reference) or Saishi et al. Applicant requests reconsideration and withdrawal of these rejections for at least the reason that none of the references describes or suggests fetching a first pair of elements, wherein the first element of the first pair of elements is a most significant element of the first pair of elements. Hoffman describes multiplying a value B of length N-bits by a value A of length 2*N-bits. Hoffman does not describe or suggest fetching a first pair of elements. Value B is an element of length-N bits and is not a first pair of elements of length 2*N-bits. Thus, Hoffman does not describe or suggest that the first element of the first pair of elements is a most significant element since value B is a single element of length N-bits. Balkanski and Saishi fail to remedy the failure of Hoffman to describe or suggest fetching a first pair of elements, wherein

the first element of the first pair of elements is a most significant element of the first pair of elements. Accordingly, Applicant requests reconsideration and withdrawal of the rejection of claim 6 for the further reason discussed above.

Claims 1-6 also stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chevillat et al. (IBM Technical Disclosure Bulletin) in view of either Balkanski et al (record reference) or Saishi et al. (record reference). Applicant requests reconsideration and withdrawal of these rejections for at least the reason that none of the references describes or suggests fetching a first pair of elements and a second pair of elements and forming a most significant product of a first element of the first pair of elements and a most significant element of the second pair of elements and a least significant product of the first element of the first pair of elements and a least significant element of the second pair of elements. Furthermore, none of the references describes or suggests shifting the most significant product left by a width of the least significant element of the second pair of elements prior to adding the most significant product to the least significant product.

Chevillat teaches a 12x16-bit multiplier capable of storing in an accumulator both the result of multiplying a 12-bit multiplier by the first 12-bits of a multiplicand and the result of multiplying the 12-bit multiplier by the last four-bits of the multiplicand. The results are scaled at the multiplied output and added in the ALU, yielding the result of the 12x16-bit multiplication. Chevillat does not describe or suggest fetching a first pair of elements and a second pair of elements and forming a most significant product of a first element of the first pair of elements and a most significant element of the second pair of elements and a least significant product of the first element of the first pair of elements and a least significant element of the second pair of elements. Chevillat's 12-bit multiplier is a single element and 16-bit multiplicand is a second pair of elements, the most significant element of the multiplicand having 12 bits and the least significant element of the multiplicand having 4 bits. Chevillat also does not describe or suggest shifting the most significant product left by a width of the least significant element of the second pair of elements prior to adding the most significant product to the least significant product. Chevillat in the Figure and page 2, third complete paragraph shows and describes a shifter. No part of Chevillat describes or suggests the number of bits shifted in the shifter and whether a left or right shift occurs. Furthermore, Chevillat describes shifting the least significant

product (second partial multiplication) and does not describe or suggest shifting the most significant product.

As explained above, Balkanski and Saishi fail to remedy the failure of Chevillat to describe or suggest fetching a first pair of elements and a second pair of elements and forming a most significant product of a first element of the first pair of elements and a most significant element of the second pair of elements and a least significant product of the first element of the first pair of elements and a least significant element of the second pair of elements. Balkanski and Saishi further fail to remedy the failure of Chevillat to describe or suggest shifting the most significant product left by a width of the least significant element of the second pair of elements prior to adding the most significant product to the least significant product.

Claims 2-6 depend from independent claim 1. Accordingly, Applicant requests that the rejections of claims 2-6 over the Chevillat, Balkanski, and Saishi references be withdrawn for the reasons discussed above with respect to claim 1.

Claim 6 describes wherein the first element of the first pair of elements is a most significant element of the first pair of elements. Claim 6 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Chevillat in view of either Balkanski et al (record reference) or Saishi et al. Applicant requests reconsideration and withdrawal of these rejections for at least the reason that none of the references describes or suggests fetching a first pair of elements, wherein the first element of the first pair of elements is a most significant element of the first pair of elements. Chevillat describes multiplying a multiplier of length 12-bits that is a single element by a multiplicand of length 16-bits that is a second pair of elements. The most significant element of the multiplicand has 12 bits and the least significant element of the multiplicand has 4 bits. Chevillat does not describe or suggest fetching a first pair of elements. The multiplier is an element of length 12-bits and is not a first pair of elements. Thus, Chevillat does not describe or suggest that the first element of the first pair of elements is a most significant element since the multiplier is a single element of length 12-bits. Balkanski and Saishi fail to remedy the failure of Chevillat to describe or suggest fetching a first pair of elements, wherein the first element of the first pair of elements is a most significant element of the first pair of elements. Accordingly, Applicant requests reconsideration and withdrawal of the rejection of claim 6 for the further reason discussed above.

Claim 9 describes a digital system having a microprocessor that can execute a rounding multiplication instruction. The microprocessor includes storage circuitry for holding pairs of elements. A multiply circuit in the microprocessor connects to receive a first number of pairs of elements from the storage circuitry in a first execution phase of the microprocessor responsive to the multiplication instruction, the multiply circuit comprising a plurality of multipliers. The microprocessor also includes an arithmetic circuit connected to receive a most significant product and a least significant product from the plurality of multipliers. The arithmetic circuit shifts the most significant product by a number of bits prior to adding the most significant product to the least significant product, the arithmetic circuit having a provision for mid-position rounding responsive to the rounding multiplication instruction. The microprocessor comprises a shifter connected to receive an output of the arithmetic circuit, the shifter operable to shift a selected amount in response to the rounding multiplication instructions.

Claims 9-11 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman in view of either Balkanski or Saishi. Applicant requests reconsideration and withdrawal of these rejections for at least the reason that none of the references describes or suggests storage circuitry for holding pairs of elements. Hoffman in Figure 1 as described above shows storage circuitry for storing a single element B of length N-bits. Balkanski and Saishi as described above fail to remedy the failure of Hoffman to describe or suggest storage circuitry for holding pairs of elements.

Claims 9-11 also stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chevillat in view of either Balkanski or Saishi. Applicant requests reconsideration and withdrawal of these rejections for at least the reason that none of the references describes or suggests storage circuitry for holding pairs of elements. Chevillat in the Figure shows a 12-bit A register and a 12-bit B register. As described in page 2 of Chevillat, 12x16 bit multiplication occurs by two steps. In Chevillat, the 16-bit multiplicand is broken up into two elements of 12 bits and 4 bits and multiplied in two different steps by the 12 bit multiplier. The first step is a 12 bit by 12-bit multiplication and the second step is a 12-bit by 4-bit multiplication. Chevillat does not describe or suggest storage circuitry for holding pairs of elements as A Register and B register are 12-bit registers that cannot store the two elements (12-bit element and 4-bit element)

of the 16-bit multiplicand. Balkanski and Saishi as described above fail to remedy the failure of Hoffman to describe or suggest storage circuitry for holding pairs of elements.

Claims 10-11 depend from independent claim 9. Accordingly, Applicant requests reconsideration and withdrawal of the rejections for claims 10-11 for the reasons discussed above with respect to claim 9.

If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at phone number (281) 207-5327.

In view of these remarks and amendments, Applicant submits that this application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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